High Performance Silicon Bipolar Power Amplifier for 1.8 GHz Applications

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Abstract — **The potential of a high-performance low-cost silicon bipolar technology for high-efficiency low-voltage RF power amplifiers has been explored. To this end, a unit power cell has been developed by optimizing layout design, collector thickness and doping level. On-wafer load-pull measurements were performed which showed an excellent power-added efficiency of 83% at 1.8 GHz under a supply voltage of 2.7 V. The optimized unit power cell was employed to implement a 1.8 GHz three-stage monolithic power amplifier. The device achieved a 57% maximum power-added efficiency and 33-dB gain at a 34-dBm output power level while operating at 2.7 V.**

I. Introduction

Extended operating time has become a fundamental requirement for battery-operated systems such as handsets for mobile communications. Power amplifiers (PAs) are the most power consuming components in portable equipment, so high power-added efficiency (PAE) is mandatory to enable long talk time and save battery life. Moreover, mobile telephones must be small and lightweight. Power amplifier supply voltage dictates the number of battery cells required which principally affects overall size and weight. Therefore, supply voltage reduction is a key design goal too.

Currently, the power amplifier market is dominated by GaAs-based modules or MMICs because of their excellent high-frequency performance even at low bias voltages. However, the drawback with these devices is a high chip cost, which in turn limits high volume production. Recently, efforts have been made to develop less expensive silicon bipolar power amplifiers for wireless applications. Outstanding results have been reported both at 900 MHz [1] and 1.9 GHz [2]. Nevertheless, a differential approach was proposed in [1] and [2] which is more sensitive to off-chip losses because it requires a rather complex lumped LC network for output power combining. Today, commercial silicon bipolar PAs are available only for less demanding systems such as DECT [3].

DCS-band performance parameters of several commercial PAs are listed in Table I for comparison purposes [4]. All of the referenced amplifiers are based on GaAs technology. None of them is able to provide an output power higher than 2 W while operating under a lower than 3 V supply voltage, and PAE values rarely exceed 50%. Power gains are lower than 30 dB. Therefore, most of the listed devices require an additional pre power amplifier (PPA) which further limits overall transmitter efficiency.

This paper presents the design and measured performance of a three-stage monolithic power amplifier for 1.8 GHz wireless communications. The chip was fabricated using a low-cost silicon bipolar technology optimized for power applications [5]. At a 2.7 V supply voltage the amplifier delivers a 34-dBm output power with 57% PAE and 33-dB gain.

Measurements show that competitive performance with existing GaAs products can be obtained by using silicon bipolar technology.

TABLE I
DCS-BAND PERFORMANCE OF COMMERCIAL POWER AMPLIFIERS

	Technology	V_{CC} [V]	P_{out} [dBm]	PAE [%]	Gain [dB]
Ericsson PBL40305	GaAs FET	3.2	31.7	41	23
Raytheon RMPA195599	GaAs HBT	3.2	32.5	50	27
Motorola MRFIC1859	GaAs FET	3.6	34	43	29
EiC ECM007	InGaP HBT	3.5	32.5	50	30
Philips CGY2014TT	GaAs FET	3.5	32.5	40	30
Anadigics AWT6107	InGaP HBT	3.5	31.5	50	24
RFMicroDevices RF3108	GaAs HBT	3.5	33	52	27
This design	**Si BJT**	**2.7**	**34**	**57**	**33**

II. Technology and Layout

The devices were fabricated in a 46-GHz-f_T double-poly 0.8 μm self-aligned-emitter silicon bipolar process by STMicroelectronics (HSB3). This is a low-cost technology which requires only 17 mask steps. It provides oxide trench isolation, three metal layers, optional gold metal layer, poly resistors, and metal-insulator-metal (MIM) capacitors with 0.7 fF/μm^2. On-chip spiral inductors are

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also available (3-μm-thick AlSiCu third metal layer) with Q values up to 9 at 1.9 GHz and resonant frequencies above 10 GHz.

In order to optimize the PAE performance of the fabrication technology a set of test devices was firstly developed and characterized. The effect of layout design on the transistor power performance was investigated. To this end, two different power transistors were fabricated and tested, one with the standard continuous narrow strip (0.8 μm) emitter and the other with a spot emitter. Mask-level spot size was set to 0.8μm × 2μm. Morcover, four process splits were carried out in order to test the effect of both collector thickness and doping concentration on transistor performance. Process splits are shown in Table II.

TABLE II
PROCESS SPLITS

Lot id.	Epi-layer thickness [μm]	Collector dose
A	1.2 (standard)	Extra light
B	1.2	Light
C	0.8	Light
D	0.8	Standard

Harmonic load-pull measurements were performed on the test devices at a 2.7-V supply voltage and a 1.8-GHz operating frequency using a single tone continuous-wave (CW) input. Harmonic load impedances were tuned for maximum PAE, i.e. an open and a short circuit were provided at the 2nd and the 3rd harmonic, respectively (dual-Class-F operation [6]-[7]). According to measurement results, the spot-emitter transistor turned out to be the most suitable one since it exhibited both higher PAE and saturated output power. Moreover, the best efficiency was achieved by reducing the epi-layer thickness to 0.8 μm and with a standard collector dose (lot D). A record 83%-PAE and a 20.4-dBm saturated CW output power were achieved at a 1.8-GHz operating frequency and a 2.7-V supply voltage, as shown in Fig. 1. The small-signal power gain was 18 dB. An excellent PAE of 75% was also obtained with a supply voltage as low as 1.8 V.

Fig. 2 shows the layout of the 48-spot-emitter optimized unit cell, which was further improved through a proper use of the higher metal layers for a better current draining.

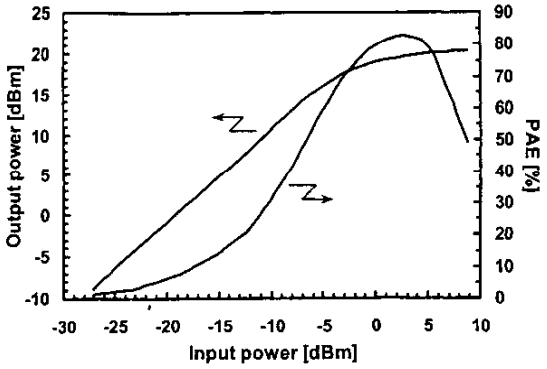

Fig. 1. Output power and PAE versus input power for the optimized unit power cell (V_{CC} = 2.7 V, f = 1.8 GHz, CW test).

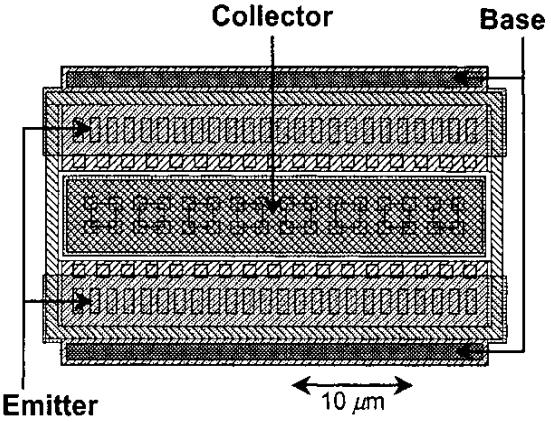

Fig. 2. Layout of the optimized unit power cell.

III. CIRCUIT DESIGN AND EXPERIMENTAL RESULTS

The optimized unit power cell was employed in implementing a monolithic PA for 1.8 GHz constant-envelope applications. Fig. 3 shows a simplified schematic of the amplifier.

The circuit is composed of three stages (*T1-T3*). Based on load-pull measurement results, a 2-cell transistor was used for the first stage, an 8-cell device for the second and a 32-cell one for the third. A bias circuit was also included which allows a power control function through the external voltage V_{CTRL}.

MIM capacitors, bondwires and a spiral inductor were used to provide on-chip interstage matching which was designed for maximum gain under large-signal conditions. Wide-band on-chip input matching was also implemented by means of an integrated resistor and a ground bondwire.

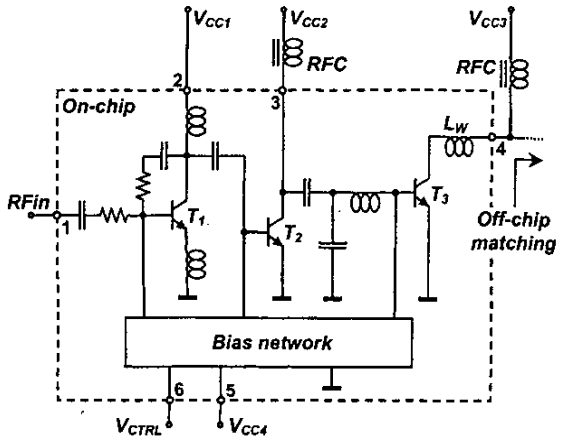

Fig. 3. Simplified schematic of the three-stage PA.

According to on-wafer load-pull measurements optimum power performance can be achieved under dual-Class-F operation, as mentioned before. Unfortunately, the implementation of a Class-F-like multi-resonant load is quite difficult at RF frequencies because of package parasitics and process tolerances. Therefore, a single-resonator solution was selected for the off-chip output matching network (only second harmonic control was performed). In such conditions, nonlinear circuit simulations showed that a good performance can be achieved when a high reactive impedance tending towards an open circuit is provided for the harmonics of the fundamental frequency, i.e. by using a series-resonant load. Such a load leads to a pulsed collector voltage and a sinusoidal collector current (mixed-C mode [7] or Class C-E [8]). Dual waveforms, i.e. pulsed current and sinusoidal voltage, are generated by a parallel-resonant load. However, such a load produces a higher current peak which causes an increased voltage drop across the collector series resistance and hence a reduction in PAE.

Fig. 4 outlines the partially distributed transformation network which was used for output matching. Bondwire inductance L_W was properly employed to provide the third stage with a series-resonant load.

A die photo of the fabricated amplifier is shown in Fig. 5. The chip size is 1.8 mm by 1.8 mm.

Measurements were performed on a 400-μm-thick FR4 substrate to conform with the low-cost production environment. The die was molded in a small 16-pin leadless plastic package which provides an exposed bottom pad for RF grounding and heat dissipation. Package size is $4 \times 4 \times 0.9$ mm. The critical emitter parasitic inductance was decreased to a suitable value by means of an on-chip ground plane (3rd metal layer) and a large number of downbonding wires.

Fig. 6 shows the output power and PAE performance versus input power at 1.8 GHz. A 57% maximum PAE was achieved at a 34-dBm output power level while operating with a 2.7-V supply voltage. The second and the third harmonics at the 50-Ω load were 45 dB and 37 dB below the carrier, respectively. Only a very small input power was required to drive the PA since the device exhibited a high 33-dB power gain under maximum PAE conditions, as well as a 41-dB small signal gain.

Fig. 7 shows the dependence of the output power and PAE on the operating frequency. It is worth mentioning that gain variation over the entire DCS transmit window (1710-1785 MHz) is less than 0.5 dB. This result comes from the use of bandwidth-optimized matching networks for process spread compensation.

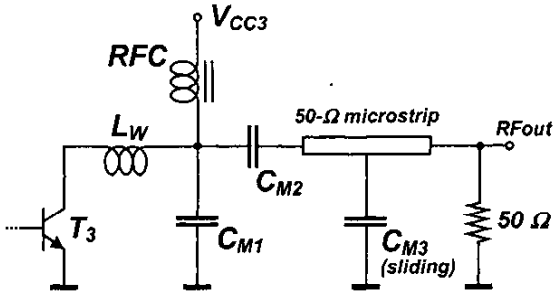

Fig. 4. Matching network at the PA output.

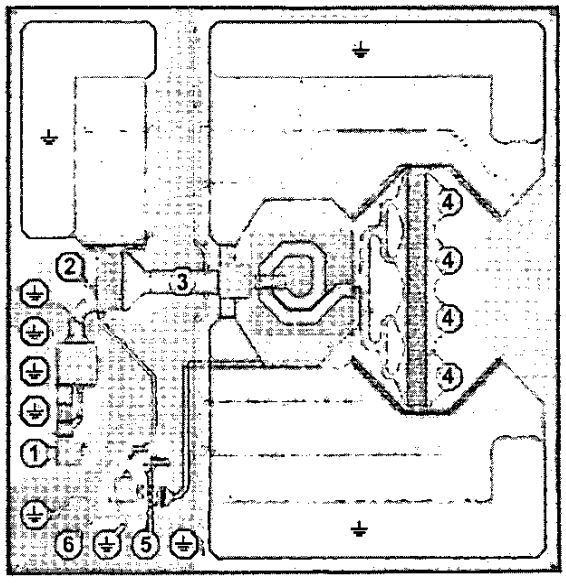

Fig. 5. Die photo of the power amplifier (see Fig. 3 for pin reference).

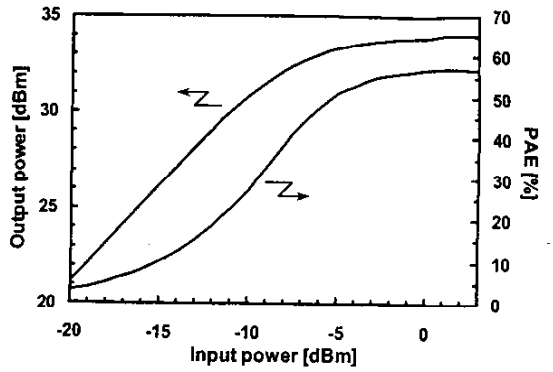

Fig. 6. Output power and PAE versus input power for the three-stage PA (V_{CC} = 2.7 V, f = 1.8 GHz, pulsed mode test).

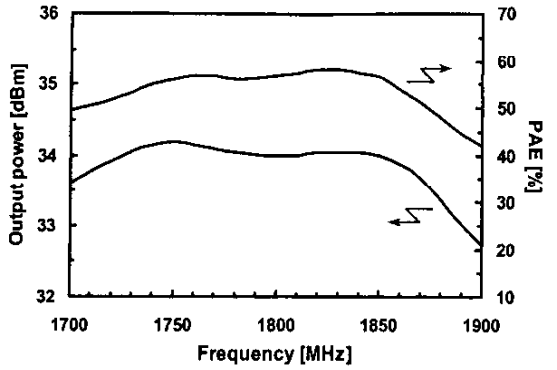

Fig. 7. Output power and PAE versus operating frequency (V_{CC} = 2.7 V, P_{in} = 1 dBm).

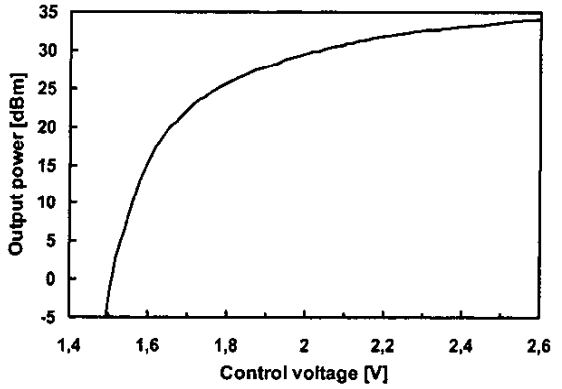

Fig. 8. Output power versus control voltage (V_{CC} = 2.7 V, f = 1.8 GHz, P_{in} = 1 dBm).

Output power versus control voltage V_{CTRL} is shown in Fig. 8. By means of the implemented bias network the power control function is successfully achieved.

IV. Conclusions

The low-voltage power capabilities of a high-performance low-cost silicon bipolar process have been investigated. By optimizing the emitter finger layout, epi-layer thickness and doping level, efficiency values up to 83% were achieved by on-wafer load-pull measurements on single-cell test devices operating at 1.8 GHz and 2.7-V power supply. Moreover, a 1.8-GHz 2.7-V three-stage monolithic power amplifier was fabricated which showed a 57% maximum PAE and 33-dB gain at a 34-dBm output power level.

These results show that silicon bipolar power amplifiers can be considered as excellent candidates for low-voltage low-consumption transmitters in mobile handsets. They amount to the best power performance reported so far for a silicon bipolar device operating in the 1.8 GHz band under a supply voltage lower than 3V.

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